IEEE Network Special Issue on Network Systems Architecture
Editorial

The last two decades have been characterized by significant advances in networking. The increasing speeds of transmission links triggered the development of a wide range of high-speed networks in the wide and local area, while the advances in access networks and mobile networking have enabled the development and deployment of network services to consumers. The prevalence of Internet technology has brought its services to a very large population, which has been growing at a geometrically increasing rate. Typical services range from digital libraries and on-line shopping to multi-player, real-time games.

The increasing requirements that new services place on networks have led to the development and deployment of complex network systems, such as switches, adapters, routers, etc., that need to execute one or more network protocol stacks. Effectively, these systems have evolved to specialized, complex computer systems composed of (possibly several) sophisticated high-speed processors, running operating systems that manage a large number of network (I/O) interfaces and executing several (possibly heterogeneous) protocols and functions. Additionally, end systems require high performance network attachments, while a large variety of end-user (consumer) network devices, such as mobile and multimedia devices, that combine processors, memory, operating systems, browsers, office applications, etc., have emerged to target a wide range of business as well as home users. Next generation consumer network devices will support pervasive and ubiquitous computing, which will be based on a huge amount of networked embedded systems, everywhere.

The demands of these network systems and appliances, in the network or at the end user premises, place significant requirements on performance and scalability as well as on other system parameters, such as power consumption, and are leading to the development of innovative architectures and components. Characteristic examples of the recent developments in this area are the innovative high-speed adapters with specialized memory managers, multiprocessor based network adapters, network processors, specialized content addressable memories, virtual output queuing switches, packet schedulers and traffic managers with quality of service support, security subsystems, etc.

Research and development targeting the architecture of these special-purpose systems is evolving as a specialized case from the field of computer architecture. Special-purpose, sophisticated architectures of network systems are necessary for the development and deployment of emerging and future networks and network services. They are required because these architectures constitute the only option for network developers who implement standardized network protocols and architectures in performance demanding environments.

As such, architectures of network systems become increasingly important to manufacturers, who seek differentiators from competitors, and to service providers, whose services can become more cost effective and scalable, when employing appropriate network systems. Importantly, the technical area of network systems architecture requires skills from networking, computer architecture, circuit design and systems software. This technical area has been emerging for the last decade and has reached the maturity necessary to be defined and identified as significant and important.

In this special issue, we include papers that address the architecture of network systems, which is not only important to industry, but to academia as well, presenting challenging research problems, that need a combination of skills in traditionally separated areas of engineering, such as networking and computer architecture. The strong interest of the research community in the area is demonstrated by the large number of submissions we received. As a result of the rigorous evaluation process, we include, finally, seven (7) papers that meet the high quality standards of IEEE Network and are fully relevant to the focus of the special issue.

The seven papers of the special issue cover several aspects of the architecture of network systems, including specific subsystems (components), distributed solutions, and service-level architectures. The first paper, “Converging the Evolution of Router Architectures and IP Networks” by A. Császár et al., argues that today’s IP network operators spend significant resources in functions like traffic engineering, policy enforcement and security because of the way control and forwarding functions are distributed among current network systems. The authors propose an architecture that alleviates the strong resource requirements and bottlenecks in the management of the Internet through centralization of network control functionality. The second paper, “Multistage Switching Architectures for Software Routers” by A. Bianco et al., proposes the deployment of ordinary PC’s in place of high-end routers; the performance and reliability limitations of PC’s are overcome by interconnecting a number of them to operate as a distributed router. Their innovative approach leads to an architecture for scalable and reliable high-speed routers.

The next paper, “Parallel Programmable Ethernet Controllers: Performance and Security” by D.L. Schuff et al., addresses the architecture of a network subsystem, a programmable 10 Gbps Ethernet controller, developing a multi-core architecture with specialized hardware support that achieves the target performance while integrating security features. The fourth paper, “Run-Time Support for Multi-Core Packet Processing Systems” by T. Wolf et al., investigates the design trade-off’s for network processor operating systems, in order to provide a run-time system that adapts dynamically to traffic pattern changes. In the fifth paper, “Path Computation Element Based Architecture for Inter-Domain MPLS/GMPLS Traffic Engineering: Overview and Performance” by S. Dasgupta et al., the authors present work performed in the Path Computation Element (PCE) Working Group at the Internet Engineering Task Force (IETF) for the path computation of inter-domain Multi-Protocol Label Switching (MPLS) and

General-MPLS (GMPLS) Label Switched Paths (TE-LSPs). The paper describes important work on an architecture that is significantly different from the traditional ones, providing also milestones and progress at the IETF PCE Working Group.

In the sixth paper, “Analysis of Shared Memory Priority Queues with Two Discard Levels” by S. Bergida and Y. Shavitt, the authors present an analytical approach to the dimensioning and management of shared memory queues. The problem arises in shared memory switches, usually deployed at network edges, which offer two rate SLA’s. Finally, the last paper of the special issue, “Improving Satellite Multicast Security Scalability by Reducing Re-keying Requirements” by V. P. Hubenko Jr. et al., attacks the problem of scalable, secure satellite multicast systems, introducing an architecture that reduces re-keying requirements, thus achieving scalability without sacrificing security. The presented solution is in the context of LEO satellite systems.

The guest editors:

- Professor Dimitrios Serpanos, University of Patras, Greece
- Professor Mario Baldi, Politecnico di Torino, Italy
- Profesor Ran Giladi, Ben Gurion University, Israel

Editors' Short Bios

Dimitrios N. Serpanos is a Professor at the Department of Electrical and Computer Engineering of the University of Patras, Greece. He holds a Ph.D. in Computer Science from Princeton University, USA, since 1990. He also holds a Diploma in Computer Engineering and Information Sciences from the University of Patras and an M.A. in Computer Science from Princeton University, since 1985 and 1988, respectively. His research interests include high-speed network systems, security systems, multimedia systems, and computer architecture.

Between 1990 and 1996, Professor Serpanos was a Research Staff Member at the IBM, T.J. Watson Research Center, USA, where he worked mainly on high-speed network systems, high-speed switches, security systems, multimedia systems and residential networks. Between 1996 and 2000, he was a faculty member (Assistant Professor and Associate Professor later) of the Dept. of Computer Science at the University of Crete, where he also worked at the Institute of Computer Science of the Foundation for Research and Technology-Hellas (ICS-FORTH). Since September 2000, he is at the Dept. of Electrical and Computer Engineering of the University of Patras, and conducts research at the Industrial Systems Institute (ISI), Patras. During his appointment in Patras, Professor Serpanos has served as Scientific Director of the Network Operations Center (NOC) of the University of Patras and he is currently Director of the Center for Computer, Network and Information Systems of the Dept. of ECE. He has worked in several research projects funded by the EU or the Greek Government. He holds close ties to industry and has led research projects funded by industry in Greece and the USA.

Professor Serpanos has received awards from IBM. He holds 2 US patents and has published numerous inventions and more than 100 scientific papers in journals and conferences. He is a Senior Member of the IEEE, a member of the New York Academy of Sciences, the ACM, and the Technical Chamber of Greece. Also, he is an educational member of USENIX.

Mario Baldi is Associate Professor of Computer Networks and head of the Computer Networks Group (NetGroup) at the Department of Computer Engineering of Politecnico di Torino (Technical University of Turin), Italy, and coordinator of the BSc programme in Information Technology Engineering and Project Manager of the Sino-Italian Engineering Campus, Tongji University, Shanghai, China.

He received his M.S. Degree Summa Cum Laude in Electrical Engineering in 1993, and his Ph.D. in Computer and System Engineering in 1998 both from Politecnico di Torino. He was Assistant Professor on tenure track at Politecnico di Torino from 1997 to 2002. He joined Synchrodyne Networks, Inc., New York, as Vice President for Protocol Architecture in November 1999.

Mario Baldi has been Honorary Visiting Professor at La Trobe University, Melbourne, Victoria, Australia, Adjunct Professor at University of Illinois at Chicago, Visiting Professor at Institut de Technologie du Cambodge, Phnom Penh, Cambodia, and visiting researcher at the IBM T. J.

Watson Research Center, Yorktown Heights, NY, at Columbia University, New York, NY, and at the International Computer Science Institute (ICSI), Berkeley, CA.

As part of his extensive research activity at Politecnico di Torino, Mario Baldi has been leading various networking research projects, involving Universities and industrial partners, funded by European Union, Local Government, and various companies, including Telecommunications Carriers, such as Infostrada and Telecom Italia, equipment vendors, such as Intel and Cisco Systems, and research institutions, such as Telecom Italia Labs and Microsoft Research.

Mario Baldi provides on a regular basis consultancy and training services, both directly to companies and through various training and network consultancy centers.

He co-authored over 70 papers on various networking related topics and two books, one (currently at the second edition) on internetworking and one on switched local area networks.

Mario Baldi is co-inventor in six patents issued by the United States Patent Office in the field of optical networking, in fourteen applications to the United States Patent Office in the fields of high performance networking and security, and one application to the European Patent Office in the field of high performance networking.

His research interests include internetworking, high performance switching, optical networking, quality of service, multimedia over packet networks, voice over IP, and computer networks in general.

Ran Giladi is an Associate Professor at the Department of Communication Systems Engineering of Ben-Gurion University, Israel. Founder of the Department of Communication Systems Engineering at Ben-Gurion University, Ran presided as its department head from 1995 until 2000. Ran co-founded several networking companies, and served in the Israeli telecom industry in many high level R&D and managerial positions. He also founded the Israeli Consortia for research on network management systems (NMS), serving as Chairman of the Consortia Board of Directors.

Ran published numerous inventions, patents and scientific papers in journals and conferences, and is on the editorial board of Telecommunication Systems Journal.

Ran acts as a Venture Partner at Tamir-Fishman Ventures, and is on the board of directors of several networking companies, among them EZchip technologies ltd., producer of state-of-the-art, ultra high speed network processors.

Ran's research includes computer and communications systems performance, data networks, and management systems. He earned a B.A. in Physics and M.Sc. in Biomedical Engineering from the Technion - Israel Institute of Technology and a Ph.D. in Computers and Information Systems from Tel-Aviv University. Ran is a Senior Member of the IEEE.